21-22

Techno Main Salt Lake
EM-4/1, Sector-V, Salt Lake City, Kolkata- 700091

Name of the Program: ***Information Technology***	**Degree:** ***B. Tech***
Course name:	**Semester:**
Course code:	**Course credit:**
Name of the student: G-1	**University roll no:**

Exp No	Name of the Experiment	Date	CO Specific Marks						Total Marks	Signature
			CO1	CO2	CO3	CO4	CO5	CO6		

Particulars of The Experiments Performed

Date	Serial No.	Experiment No.	Subject / Experiment	Page No.	Signature	Remarks

Techno Main Salt Lake
EM-4/1, Sector-V, Salt Lake City, Kolkata- 70009

Institute Vision:

Emerge as a centre of excellence for engineering and management studies encouraging research and building leaders contributing towards individual and social empowerment.

Institute Mission:

- To identify individual potential, capabilities and skills to achieve confidence and competence.
- To practice innovative and modern methods of pedagogy encouraging holistic education and research.
- To enhance employability skills through collaborative ventures with the industry.
- To build leaders and entrepreneurs with integrity and ethics fostering growth and sustainability.

Departmental Vision:

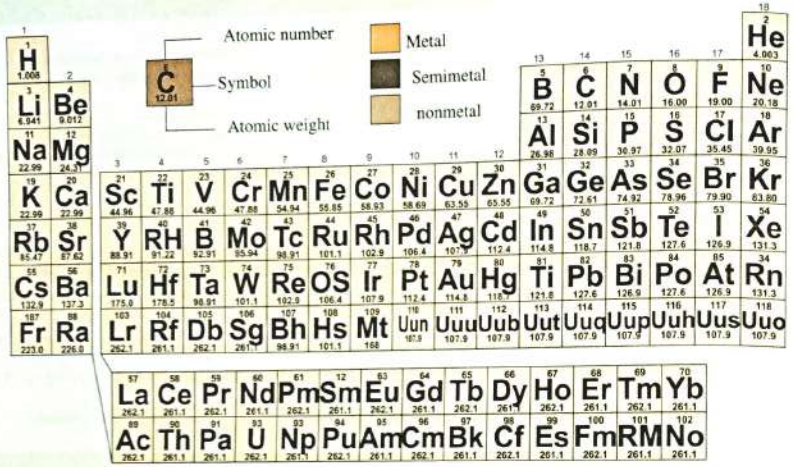
To nurture and motivate students towards imbibing the essentials of Information Technology and explore their potentials in IT industries & ITeS for addressing societal causes.

Departmental Mission:

- ❖ To develop students as well-nurtured IT professionals through devoted facilitators and enthusiastic alumni.
- ❖ To provide training on emerging technologies thereby enabling the students' industry ready.
- ❖ To inspire students in research on niche areas through innovative practices, development and modelling.
- ❖ To encourage students in lifelong learning for exploring multidisciplinary interactions of IT in societal needs.
- ❖ To groom up leadership and entrepreneurial skills in the aspiring engineers.

Brown : - PbO_2, CuO, Fe_2O_3, FeO_4, Ag_3AsO_4, ...
Black : - PbS, CuS, CuO, Bi_2SI_3, FeO, CoO, NiO, HgS, FeS, MnO_2, Co_3O_4, CoS, Nis, Ni_2O_3, Ag_2S.
Orange Red : Dichromates, Sb_2S_3.

Periodic Table



SIMPLE COLOURED IONS IN SOLUTIONS

Blue : - Cu^{2+} Green : - Fe^{2+}, MnO_4^{2-}, Cr^{3+}, Ni^{2+}, $Fe(CN)_6^{4-}$, Fe^{3}
Pink : - CO^{2+}, Mn^{3+}, Putple : - MnO_4^{3-}, Orange Red : $Cr_2O_7^{2-}$.
N.B. : Coloured ions are best seen in dilute solutions. Yellow colour is often observed in conc. HCl and aquaregia solutions.

Strength of some common Acids and of Ammonium Hydroxide

	APPROXIMATE			Vol. required to make
	Sq. Gr.	% by wt.	Normality	1 litre N (app) Soln.
Acetic acid, glacial	1.05	99.5	17.4	58 c.c.
Hydrochloric acid	1.18	35.0	11.3	89 ,,
Nitric acid	1.42	69.8	16.0	63 ,,
Phosphoric acid	1.69	85.0	14.7	23 ,,
Sulphuric acid	1.84	96.0	36.0	28 ,,
Ammonium Hydroxid	0.90	27 (NH_3)	14.3	71 ,,

Some commons Laboratory Reagents Dilute solution of acid and alkalies

Reagent	Normality	Amount per litre
Acetic acid	5	285 gms
Hydrochloric acid	5	480 gms
Nitric acid	5	310 gms
Sulphuric acid	5	140 gms
Ammonium hydroxide	5	338 gms
Potassium hydroxide	5	310 gms
Sodium hydroxide	5	220 gms

Course Objectives:

This course equips students to grasp the VHDL programming language, navigate the Xilinx ISE design suite, and simulate digital circuits within the ISE environment, fostering a comprehensive understanding of digital circuit design and implementation.

Course Outcome:

On completion of the course, students will be able to:

PCC-CS492.1	Apply modern development tools to design complex digital circuits
PCC-CS492.2	Analyze syntax and behavior of the VHDL
PCC-CS492.3	Develop the combinational and sequential logic circuits using VHDL
PCC-CS492.4	Design simple ALU and CPU using VHDL

blue litmus paper turns red at an acide pH of about 8. Neither changes colour if the pH is nearly neutral. Litmus is an organic compound derived from lichens.
Phenolpthalein is also a common indicator, being colourless isn solution at pH below 8 and turning pink for pH above.

Name of the Program: *Information Technology*	Course Code:
Semester:	Course Name:
Name of the student:	University roll no:
Name of the Experiment:	
Objective of the Experiment:	
Date of the Experiment:	

Quality/ Score ⟹ / Objective/ Criteria ⇩	Excellent (4)	Good (3)	Fair (2)	Poor (1)	
Lab participation (Lab technique /subject knowledge / contribution)					
Lab Report (Diagram/ Calculation/ Graph/ QA)					
Execution & Debugging (Usage of tools)					
Discipline in Lab (Discipline/ Cooperation/ Cleanliness/ Rearranging after experiment)					
Lab performance based Viva Voce					
Total Marks (out of 20)					/ 20
Remarks (if any)					
Signature of the faculty with date					

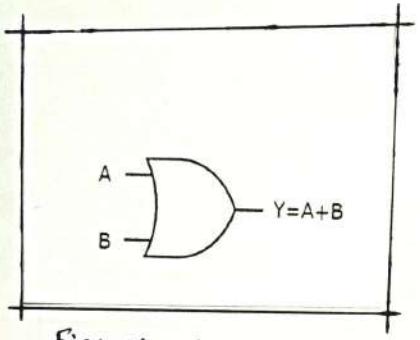


Fig: Circuit Diagram

Topic: Experiment-1.1

PIONEER
Page:
Date: / /

Objective: Implementation of OR Gate using VHDL.

Truth Table:

Inputs		Output
A	B	Y
0	0	0
0	1	1
1	0	1
1	1	1

VHDL Source Code:

```
library IEEE;
use IEEE.std_logic_1164.all;
entity orGate is
    port(A : in std_logic;
         B : in std_logic;
         Y : out std_logic);
end orGate;
architecture orLogic of orGate is
begin
    Y <= A OR B;
end orLogic;
```

Test Bench Waveform:

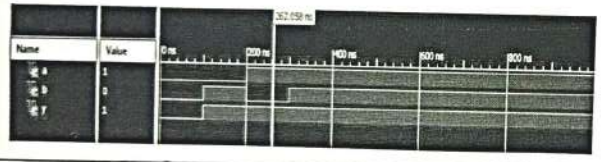


Fig: Test Bench Waveform.

Topic :

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VHDL TestBench Code :

```
LIBRARY ieee;
USE ieee.std_logic_1164.ALL;
ENTITY TESTORGATE IS
END TESTORGATE;
ARCHITECTURE behavior OF TESTORGATE IS
  COMPONENT ORGATE
  PORT(
    A : IN std_logic;
    B : IN std_logic;
    Y : OUT std_logic);
  END COMPONENT;
  Signal A: std_logic := '0';
  Signal B: std_logic := '0';
  Signal Y : std_logic;
  BEGIN
    uut: ORGATE PORT MAP(
      A => A, B => B, Y => Y);
    stim_proc: process
    begin
      A <= '0'; B <= '0'; Wait for 100 ns;
      A <= '0'; B <= '1'; Wait for 100 ns;
      A <= '1'; B <= '0'; Wait for 100 ns;
      A <= '1'; B <= '1'; Wait for 100 ns;
    Wait; end process;
END;
```

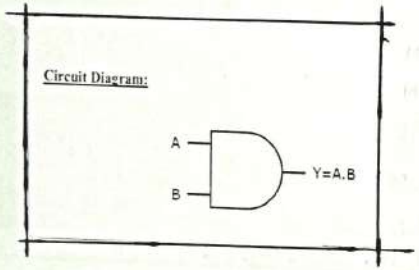

Fig: Circuit Diagram.

Topic: Experiment-1.2

Page:

Date: / /

Objective: Implementation of AND gate using VHDL.

Truth Table:

Inputs		Outputs
A	B	Y
0	0	0
0	1	0
1	0	0
1	1	1

VHDL Source Code:

```
library IEEE;
use IEEE.std_logic_1164.all;
entity andGate is
  port(A: in std_logic;
       B: in std_logic;
       Y: out std_logic);
end andGate;
architecture andLogic of andGate is
begin
  Y <= A AND B;
end andLogic;
```

VHDL Test Bench Code:

```
LIBRARY ieee;
USE ieee.std_logic_1164.ALL;
```

Test Bench Waveform:

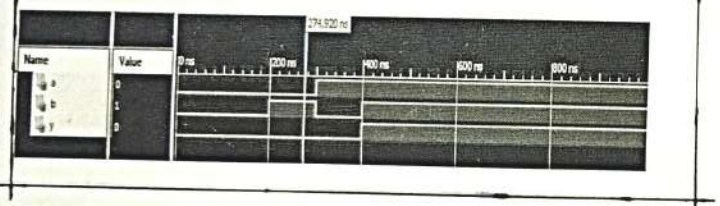

Fig: Test Bench Waveform.

Topic :

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Date : / /

```
ENTITY TESTANDGATE IS
END TESTANDGATE;
ARCHITECTURE behavior OF TESTANDGATE IS
  COMPONENT ANDGATE
  PORT( A : IN std_logic; B : IN std_logic;
        Y : OUT std_logic);
  END COMPONENT;
  Signal A : std_logic := '0';
  Signal B: std_logic := '0';
  Signal Y: std_logic;
  BEGIN
    uut : ANDGATE PORT MAP(
          A => A, B => B, Y => Y);
    Stim_proc : process.
    begin
      Wait for 100 ns;
      A <= '0'; B <= '0'; Wait for 100 ns;
      A <= '0'; B <= '1'; Wait for 100 ns;
      A <= '1'; B <= '0'; Wait for 100 ns;
      A <= '1'; B <= '1'; Wait for 100 ns;
    Wait;
    end process;
  END;
```

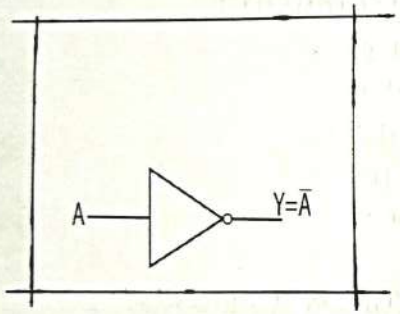

Fig: Circuit Diagram.

Topic: Experiment - 1.3

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Page :

Date : / /

Objective: Implementation of NOT Gate using VHDL.

Truth Table:

Inputs	Output
A	Y
0	1
1	0

VHDL Source Code:

```
library IEEE;
use IEEE.std_logic_1164.all;
entity notGate is
 port (A : in std_logic;
       Y : out std_logic);
end notGate;
architecture notLogic of notGate is
 begin
   Y <= NOT A;
 end notLogic;
```

VHDL TestBench Code:

```
LIBRARY ieee;
USE ieee.std_logic_1164.ALL;
ENTITY TESTNOT IS
 END TESTNOT;
ARCHITECTURE behavior OF TESTNOT IS
 COMPONENT NOTGATE
```

Test Bench Waveform:

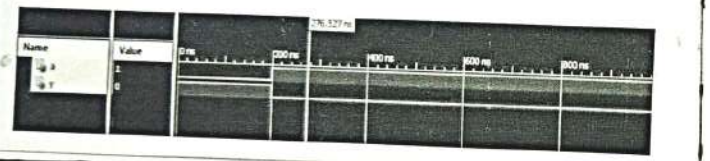

Fig: Test Bench Waveform.

```
PORT ( A : IN std_logic ;
       Y : OUT std_logic );
END COMPONENT ;
  signal A : std_logic := '0';
  signal Y : std_logic ;
  BEGIN
     uut : NOTGATE PORT MAP (
          A => A, Y => Y );
   stim_proc : process
   begin
     wait for 100 ns ;
      A <= '0' ; wait for 100 ns ;
      A <= '1' ;
      wait ;
    end process ;
   END ;
```