

Computer Architecture Lab [IT592/PCC-CS492]

LAB MANUAL

V & IV SEMESTER



Department of Information Technology
Techno Main Salt Lake
EM 4/1 Salt Lake, Sec – V, Kolkata – 700091.

1. Course Information:

NAME OF THE PROGRAM: <i>Information Technology</i>	DEGREE: <i>B. Tech</i>
COURSE NAME: <i>Computer Architecture</i>	SEMESTER: <i>5th & 4th</i>
COURSE CODE: <i>IT 592 & PCC-CS 492</i>	COURSE CREDIT: <i>2</i>
COURSE TYPE: <i>Lab Manual</i>	CONTACT HOURS: <i>4L</i>

2. Institute Vision:

Emerge as a center of excellence for engineering and management studies encouraging research and building leaders contributing towards individual and social empowerment.

3. Institute Mission:

- ❖ To identify individual potential, capabilities and skills to achieve confidence and competence.
- ❖ To practice innovative and modern methods of pedagogy encouraging holistic education and research.
- ❖ To enhance employability skills through collaborative ventures with the industry.
- ❖ To build leaders and entrepreneurs with integrity and ethics fostering growth and sustainability.

4. Departmental Vision:

Nurture and motivate students to actively learn the concepts of Information Technology to explore their potentials in IT industry and innovate through new ideas for society.

5. Departmental Mission:

- ❖ To inculcate training on emerging technologies and making them industry ready.
- ❖ To inspire their creativity in research through innovative development and modelling.
- ❖ To groom up their leadership skill for emerging as an entrepreneur.
- ❖ To develop well nurtured IT professionals through devoted facilitators and enthused alumni.
- ❖ To encourage in lifelong learning for exploring multidisciplinary interactions of IT in societal needs and boost up entrepreneurial skills.

6. Program Educational Objectives (PEOs):

PEO1: The graduates will contribute to society as educated, expressive, ethical and responsible citizens with proven expertise.

PEO2: Individuals who will achieve peer-recognition - as an individual or in a team through demonstration of good analytical and implementation skills in IT-based projects and otherwise.

PEO3: The graduates will pursue higher education, research and development and other creative and innovative efforts, including entrepreneurship.

PEO4: The graduates will be able to demonstrate sustained learning and adapt to a constantly changing world through professional development and self-study.

7. Program Outcomes (POs):

PO1: Engineering knowledge: Apply the knowledge of mathematics, science, engineering fundamentals, and an engineering specialization to the solution of complex engineering problems.

PO2: Problem analysis: Identify, formulate, review research literature, and analyze complex engineering problems reaching substantiated conclusions using first principles of mathematics, natural sciences, and engineering sciences.

PO3: Design/development of solutions: Design solutions for complex engineering problems and design system components or processes that meet the specified needs with appropriate consideration for the public health and safety, and the cultural, societal, and environmental considerations.

PO4: Conduct investigations of complex problems: Use research-based knowledge and research methods including design of experiments, analysis and interpretation of data, and synthesis of the information to provide valid conclusions.

PO5: Modern tool usage: Create, select, and apply appropriate techniques, resources, and modern engineering and IT tools including prediction and modeling to complex engineering activities with an understanding of the limitations.

PO6: The engineer and society: Apply reasoning informed by the contextual knowledge to assess societal, health, safety, legal and cultural issues and the consequent responsibilities relevant to the professional engineering practice.

PO7: Environment and sustainability: Understand the impact of the professional engineering solutions in societal and environmental contexts, and demonstrate the knowledge of, and need for sustainable development.

PO8: Ethics: Apply ethical principles and commit to professional ethics and responsibilities and norms of the engineering practice.

PO9: Individual and team work: Function effectively as an individual, and as a member or leader in diverse teams, and in multidisciplinary settings.

PO10: Communication: Communicate effectively on complex engineering activities with the engineering community and with society at large, such as, being able to comprehend and write effective reports and design documentation, make effective presentations, and give and receive clear instructions.

PO11: Project management and finance: Demonstrate knowledge and understanding of the engineering and management principles and apply these to one's own work, as a member and leader in a team, to manage projects and in multidisciplinary environments.

PO12: Life-long learning: Recognize the need for, and have the preparation and ability to engage in independent and life-long learning in the broadest context of technological change.

8. Program Specific Outcomes (PSOs):

PSO1: Ability to apply concepts of Information Technology in industrial applications.

PSO2: Ability to innovate new ideas to boost research and development.

PSO3: Ability to adapt with upcoming technological changes.

9. Syllabus:

Laboratory Experiments:	
1	HDL introduction
2	Basic digital logic base programming with HDL
3	8-bit Addition, Multiplication, Division
4	8-bit Register design
5	Memory unit design and perform memory operations.
6	8-bit simple ALU design
7	8-bit simple CPU design
8	Interfacing of CPU and Memory

10. Text Book, Reference Book and Special Resources:

Text Books:

11. Course Objectives:

12. Course Outcome:

On completion of the course, students will be able to:

PCC-CS 402.1	Learning pipelining concepts with a prior knowledge of stored program methods.
PCC-CS 402.2	Learn about memory hierarchy and mapping technique.
PCC-CS 402.3	Study of parallel and interconnection network.

13. System Specifications:

Hardware Specification

- Core i3
- RAM – 4 GB
- HDD – 500 GB

Software Specification

- Xilinx ISE Design Suit

14. Code of conduct:

1. All students must observe the Dress Code while in the laboratory.
2. Sandals or open-toed shoes are NOT allowed.
3. Foods and drinks are NOT allowed.
4. All bags must be left at the indicated place.
5. Be PUNCTUAL for your laboratory session.
6. Experiment must be completed within the given time.
7. Noise must be kept to a minimum.
8. Handle PC with care.
9. Do not use any external device without prior permission.
10. Do not use Mobile Phone inside Laboratory.
11. All students are liable for any damage due to their own negligence.
12. Students are strictly PROHIBITED from taking out any items from the laboratory.
13. Report immediately to concern teachers if any injury occurred.
14. Report immediately to concern teachers any damages to equipment.
15. Report immediately to concern teachers if any malfunction found in hardware devices.

Before leaving the laboratory:

1. Place the chairs at proper place.
2. Turn off the power to PC properly.
3. Please check the laboratory notice board regularly for updates.

15. Topics:

CONTENTS

SL. NO.	EXPERIMENT NAME	PAGE NO.
1	HDL introduction	
2	Basic digital logic base programming with HDL	
	Implementation of OR Gate using VHDL.	
	Implementation of AND Gate using VHDL.	
	Implementation of NOT Gate using VHDL.	
	Implementation of XOR Gate using VHDL.	
	Implementation of XNOR Gate using VHDL.	
	Implementation of NOR Gate using VHDL.	
	Implementation of NAND Gate using VHDL.	
	Design of the Boolean function $F = AC + \overline{A}B + \overline{A}BC + \overline{B}C$.	
3	8-bit Addition, Multiplication, Division	
	Implementation of Half-Adder using VHDL.	
	Implementation of Full-Adder using VHDL.	
	Implementation of Half-Subtractor using VHDL.	
	Implementation of Full-Subtractor using VHDL.	
	Implementation of Full Adder Using Two Half Adder using VHDL.	
	Implementation of Full Subtractor Using Two Half Subtractor using VHDL.	
	Implementation of 8-Bit Full Adder Using VHDL Program.	
	Implementation of 4 Bit Adder-Subtractor Composite Circuit using VHDL.	
	Implement 8 bit multiplication/Division circuit using Data Flow Architecture.	
4	Design and implement a 2:1 MUX, 4:1 MUX and 8:1 MUX circuit in VHDL using Data Flow/ Behavioural Model.	
	Design and implement a 4:1 MUX using 2:1 MUX circuit in VHDL using Structural Model	
	Design and implement 1:16 DEMUX circuit in VHDL using Data Flow and Behavioural Architecture.	

	Design and implement a Decoder (2X4) circuit in VHDL using Behavioural Architecture.	
5	Design and implement SR, JK, T and D Flip Flop circuit in VHDL using Behavioural architecture.	
	Implementation of SR Flip Flop circuit in VHDL using Behavioural architecture.	
	Implementation of JK Flip Flop circuit in VHDL using Behavioural architecture.	
	Implementation of T Flip Flop circuit in VHDL using Behavioural architecture.	
	Implementation of D Flip Flop circuit in VHDL using Behavioural architecture.	
	Implement Up and Down counter using Flip Flop in VHDL using Behavioural architecture.	
	Implementation of 8-bit Register Using VHDL	
6	Implementation of Memory unit design and perform memory operations.	
7	Design a 4 bit ALU capable of doing all basic arithmetic and Logical operations.	
8	8-bit simple ALU design	
9	8-bit simple CPU design	
10	Interfacing of CPU and Memory	